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ABSTRACT

Euclid is the ESA mission to map the geometry of the dark Universe using two cosmological probes, namely Weak Lensing and Baryonic Acoustic oscillations. The visual imager, a CCD based optical imaging channel will be used to measure the shapes of galaxies in one single wide visual band spanning the wavelength range of 550-920 nm. The focal plane array supports 36 CCDs (4k×4k pixels each) with 0.101 arcsec pixel platescale, giving a geometric field of 0.55 deg^2. With the weak lensing technique, the mass distribution of the lensing structures can be traced back.

The originally baselined CCDs were e2v CCD203-82. Following the results from a dedicated radiation damage test activity on their CCD204 variant, a new version, called 273 has been designed and made available in a front-illuminated version in April 2012.
For Euclid, the accuracy with which the shape of the galaxies has to be measured is considerable: 1% and has never been demonstrated. The radiation damage effects will adversely affect this measurement and thus need to be characterized. Therefore, several test campaigns on the characterization of the CCD radiation damages for Euclid are carried out by ESA and by the Euclid Imaging Consortium.
For this purpose, a test bench has been implemented at ESTEC to characterize CCD devices, with radiometric measurements, point source illumination and lab simulation of typical Euclid sky images. The preliminary results obtained at ESA on a non-irradiated front-illuminated Euclid prototype CCD 273-84-2-F16 will be shown in this article.

Keywords: Euclid, dark energy, dark matter, CCD

1. INTRODUCTION

Euclid is the ESA mission to map the geometry of the dark Universe using two cosmological probes, namely Weak Lensing and Baryonic Acoustic oscillations. The mission will observe galaxies and clusters of galaxies out to a red-shift of z~2, in an all-sky survey covering 15 000 deg². It consists of a 1.2m diameter telescope with two focal plane instruments provided by the Euclid Mission Consortium: a visual imager (VIS) and a near-infrared spectrometer-photometer (NISP).

The visual imager, a CCD based optical imaging channel will be used to measure the shapes of galaxies in one single wide visual band spanning the wavelength range of 550-920 nm, with about 0.16 arcsec (FWHM) system point-spread function excluding pixelisation. The focal plane array supports 36 back-illuminated CCDs (4k×4k pixels each) with 0.101 arcsec/pixel plate scale, giving a geometric field of 0.55 deg^2. With the weak lensing technique, the mass distribution of the lensing structures can be traced back.

The originally baselined CCDs were e2v CCD203-82. As a test vehicle the 1kx4k variant CCD204 was used in a dedicated radiation test campaign. Based on the results from this test activity (led by SSTL, UK), a new version, called CCD273 has been designed and made available in a front-illuminated version in April 2012. For Euclid, the accuracy with which the shape of the galaxies has to be measured is considerable: 1% and has never been demonstrated. The radiation damage effects will adversely affect this measurement and thus need to be characterized.

Therefore, several test campaigns on the characterization of the CCD radiation damages for Euclid are carried out by ESA and by the Euclid Imaging Consortium.

For this purpose, a test bench [1] has been implemented at ESTEC to characterize CCD devices, with radiometric measurements, point source illumination and lab simulation of typical Euclid sky images. The preliminary results obtained at ESA on a non-irradiated CCD 273-84-2-F16 will be shown in this article, including bias, clocking scheme and noise optimization.

2.   DESCRIPTION OF THE DETECTOR

2.1 Architecture

The CCD 273-84-2-F16 [2] is a front-illuminated Euclid format device delivered to ESA as part of the Euclid CCD predevelopment contract phase 1. In phase 2 of this contract, back-illuminated versions of this device will be fabricated. It is a device with 4k x 4k pixels, divided in two halves with a charge injection structure in the middle. Each of the two read-out registers has two output nodes, one at either end.
It is based on the existing CCD203-82 design with some changes and trade-offs to optimise performance :
-    there is only one output gate at the end of each read-out register, which eliminates the option of gain switching
-    the width of the register channel has been reduced to improve the radiation hardness of the device
-    a parallel charge injection structure has been included in the middle of the device,
-    and a high resistivity silicon and a thin gate dielectric processes were chosen.
-    The output amplifier is derived from the output amplifier of CCD231, and combines low noise and high responsivity (~7-8 μV/e-).
The read-out register has a gate controlled dump drain to allow fast dumping of unwanted data.

The SiC package provides guaranteed flatness at cryogenic temperatures, as well as a compact footprint. Connections are made at the top and bottom of the device, so that the sides may be close butted if needed. The end-bonded flexis at the top and bottom are made such that close butting is also possible at the end-to-end side. The devices do not have a cover window.

Devices are intended for operation at cryogenic temperatures, where the dark signal is negligible, and are tested at the nominal Euclid operating temperature of 153K (-120°C), but can function correctly down to about 133K (-140°C), the onset of carrier freeze-out causing loss of transfer efficiency.

The topology of the CCD is shown in Figure 1. View is through the silicon, from the back-thinned side.
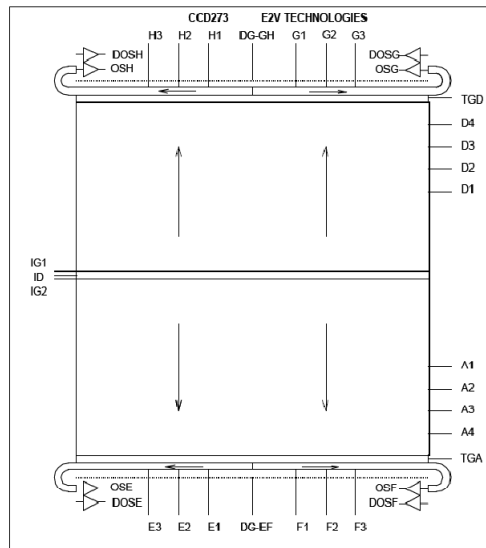

Figure 1: Layout schematic of CCD273.

In order to enable the testing of the device in our set-up, a new cold stage was built out of Ti, replacing the Al cold stage dedicated to CCD204 testing. This was done to provide a better match in the Coefficient of Thermal Expansion with the SiC package of the CCD273. The FEE headboard for CCD204 testing was used with only a minor modification to provide Vid to the CCD273. As a consequence of using this headboard, only one half of the CCD can be biased and readout. Because of the hardwired connection of the parallel transfer gate (TG) to one of the image clock phases, it was only possible to readout image section D. Both amplifiers G and H can be read out, but only one at a time.

We use a single channel CDS card with Dual Slope Integration and a 16 bits ADC (XCAM ltd, UK).

The CCD was illuminated with a [55]Fe source (shutter controlled), typical exposure time was 2 seconds. Most tests were done at T=153K, the baseline operating temperature of the CCDs on Euclid. Temperature is measured from a PT1000 sensor glued in a threaded holder, which in turn is mounted in one of the spare M2.5 inserts in the back of the SiC package. The temperature sensors provided by e2v on the SiC package have not been used, since our headboard wiring is not compatible with T-sensor readout.

2.2 Clocking scheme

The device has 4-phase image electrodes and a 3-phase serial register. It can be operated in a full-frame mode with read-out from either one or two outputs. The actual drive pulses, R1, R2, R3 for the register and the CDS timing, are as specified in the subsequent timing diagram, shown in Figure 2.
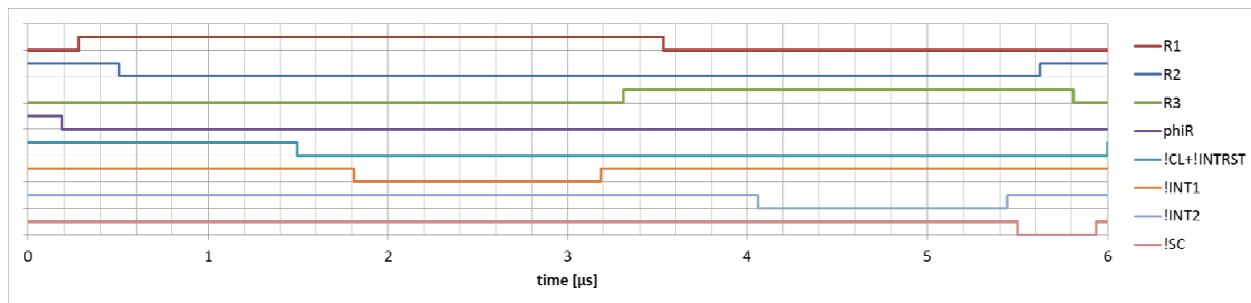

Figure 2: Clocking scheme for pixel readout at 167 kHz. Clock phases R1-R3 overlap by ~ 200 ns.

We use a clocking scheme with ~200ns overlap of the serial clock phases. Compared to CCD204 read-out, we had to introduce an extra ~0.5 µs delay before the first CDS integration period (!INT1 in Figure 2) in order to reduce the noise by a factor of 3-4. The pixel readout time is now consisting of:
- 3.5 µs overhead of clocking and delays,
- $2*T_{int}$, the two CDS integration periods.

Hence, the maximum pixel rate amounts to 285 kHz (with infinitely short CDS integration time). We distinguish between pixel rate (the inverse of the pixel read out time) and CDS frequency (defined as $1/(2*T_{int})$). While noise versus pixel rate is obviously the relevant relationship for an application, the noise performance is more related to the CDS frequency or integration time.

The noise results in the section below will be shown as a function of both parameters.

3.   BIAS OPTIMISATION

3.1 Optimizing the output drain and reset voltages

The schematics for the output circuit is shown in Figure 3 and the Table 1 summarizes the various bias voltages.
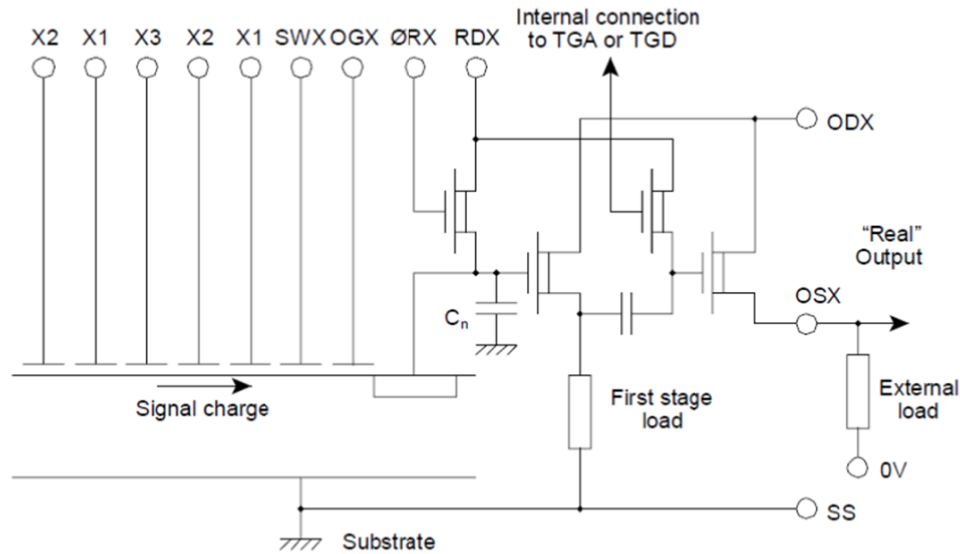
Figure 3: Schematic of the output circuit.

Table 1: Reference list of the various bias voltages.

Reference	Parameter
$R\phi$	Register clock phase
$I\phi$	Image clock phase
TG	Transfer Gate
V_{od}	Output Drain
V_{og}	Output Gate
ϕR	Reset Gate
V_{rd}	Reset Drain
V_{dd}	Dump Drain
V_{dg}	Dump Gate
V_{id}	Injection Drain
V_{ig}	Injection Gate
V_{ss}	Substrate

The bias voltages V_{od} (output drain) and V_{rd} (reset drain) have been optimised with respect to noise and gain stability. For this purpose a test matrix with $V_{od} = 23\text{-}29$ V and $V_{rd} = 12\text{-}19$ V in steps of ~ 0.5V has been explored. The results are shown in Figure 4 (amplifier H) and Figure 5 (amplifier G) It should be noted that the measurements for amplifier G suffered from the pressure gauge on the cryostat being switched on, resulting in excess noise

The noise calibration from ADUs to electrons was done from the Mn-Kα peak in the spectrum. We assumed an average of 1577.5 electrons from a single Mn-Kα photon (E=5895 eV) at T=153K. No correction was applied for charge loss due to finite CTI. (In our tests, the application of such a correction would reduce the noise by typically 1%).

The voltages after optimization are listed in Table 2. Note that at this stage, no optimization of clock levels was done.
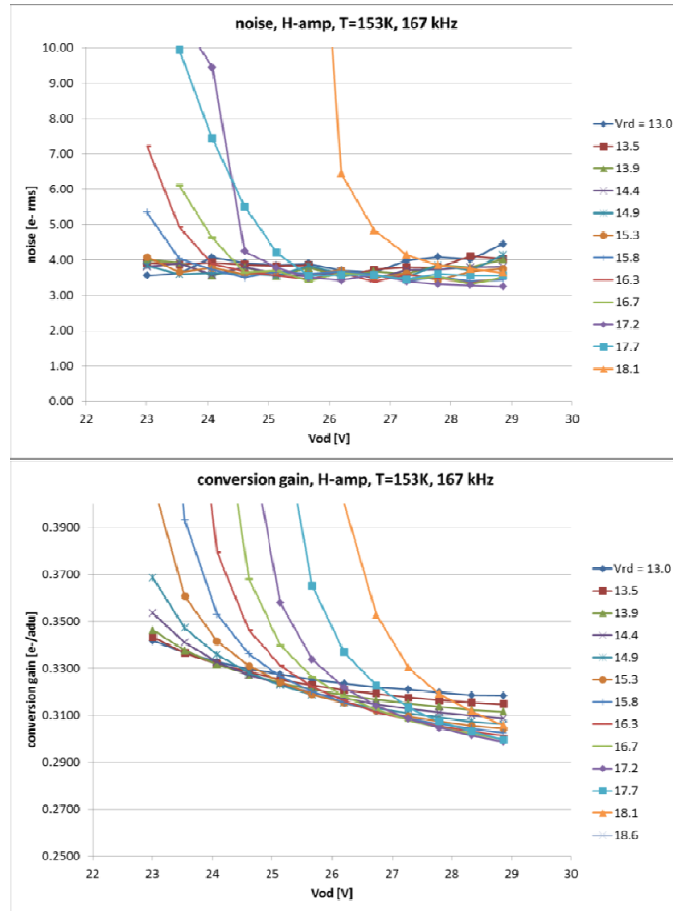
Figure 4: Measured noise (top) and conversion gain (bottom) as a function of V_{od} and V_{rd} for amplifier H. Pixel rate was 167 kHz, CDS rate was 400 kHz, T=153 K.
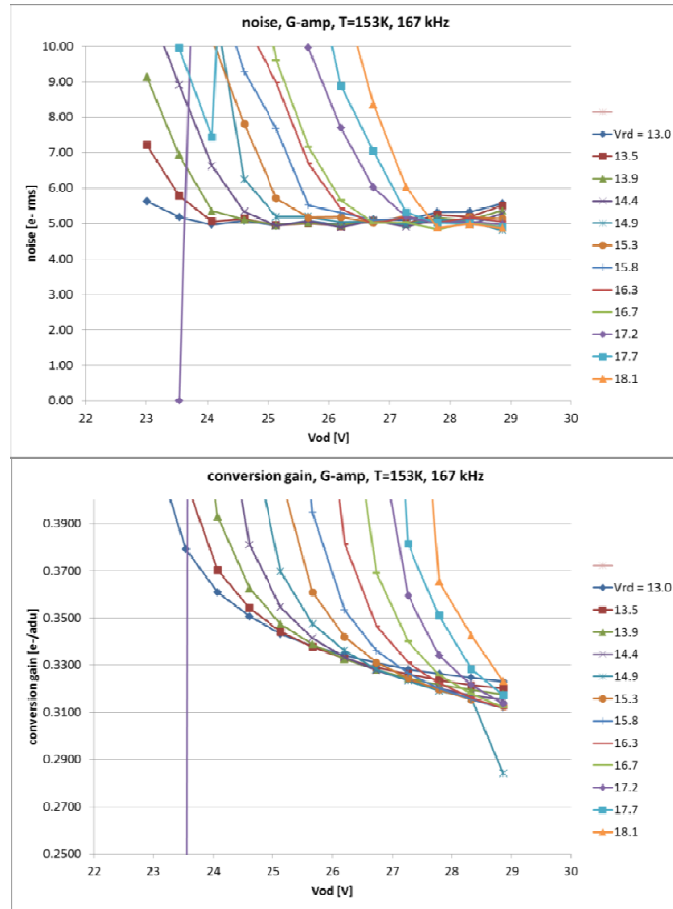
Figure 5: Measured noise (top) and conversion gain (bottom) as a function of V_{od} and V_{rd} for amplifier G. Pixel rate was 167 kHz, CDS rate was 400 kHz, T=153 K. Noise is higher compared to amplifier H due to a pressure gauge being ON during the measurements.

Table 2: Bias voltages after optimisation for amplifiers G and H. All clock low levels are 0V. The 3rd column lists the optimum voltages obtained after further optimisation described in section 3.2 and 3.3.

Parameter	[V] during bias optimisation	[V] final values
Rϕ high	9.0	8.5
Iϕ high, TGD high	9.0	11.5
ϕR high	9.0	8.5
V_{od}	23-29	26.7/26.3
V_{rd}	12-19	16.3
V_{og}	2.0	2.0
V_{dd}	20.0/23.0	18.0
V_{id}	23.0	20.0
V_{ig} high	9.0	8.5
V_{ss}	0	0

3.2 Optimizing the reset pulse amplitude

In order to find the proper value of the reset pulse high level ϕR_H, the noise and conversion gain were measured from 2s exposures to ^{55}Fe x-rays. Results are shown in Figure 6. While the measured noise is found independent of ϕR_H, the conversion gain is not stable for $\phi R\_H < 8V$, indicating that the readout node is not properly reset. For further operations a value of $\phi R\_H = 8.5V$ is adopted.
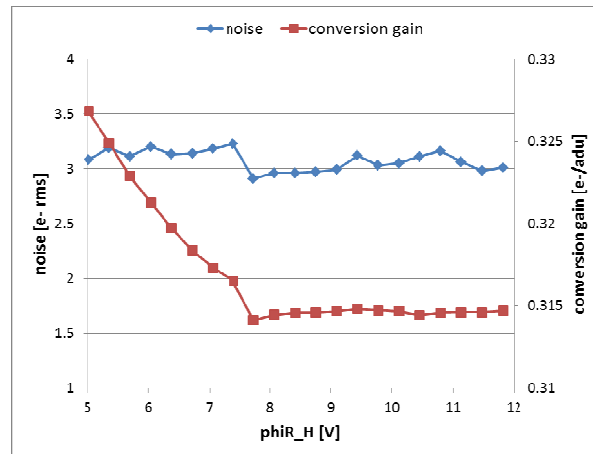

Figure 6: Noise and conversion gain as a function of the reset pulse amplitude ϕR_H (readout through amplifier H).

3.3 Noise versus register and image clock amplitudes

An elaborate matrix of noise measurements with clock amplitudes $R\phi\_H = 7.0\text{-}11.7V$ and $I\phi\_H = 8.0\text{-}11.8V$ was performed, the results of which are shown in Figure 7. The temperature was 153K and the pixel rate was 167 kHz.
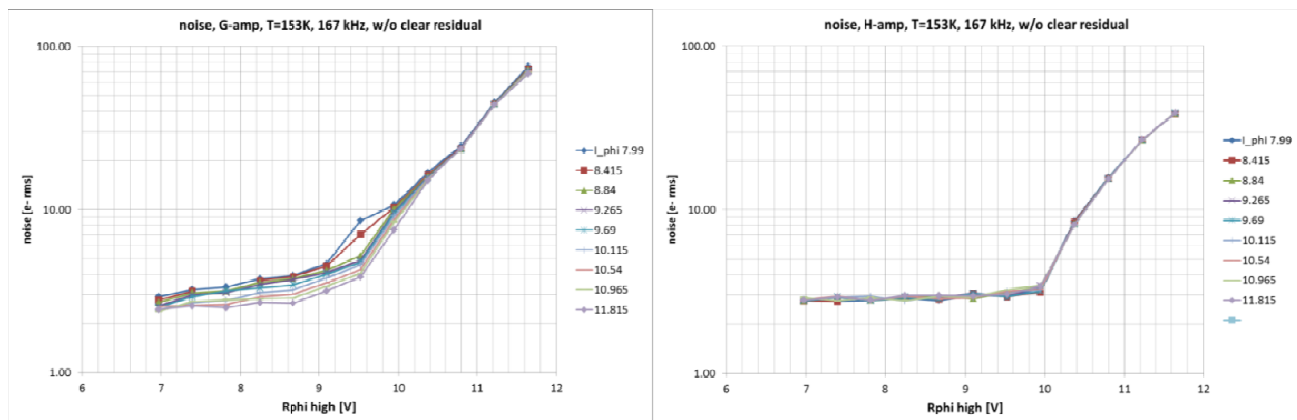

Figure 7: Noise as a function of $R\phi\_H$ and $I\phi\_H$, for amplifier G (left) and amplifier H (right).

For amplifier H, the noise is completely independent of $I\phi\_H$, and almost independent of $R\phi\_H$ for values <10.0V. For higher values, the noise increases rapidly For amplifier G, this is quite different: for $R\phi\_H < 10.0V$, the noise improves with increasing $I\phi\_H$, and degrades with increasing $R\phi\_H$. For $R\phi\_H > 10.0V$, the behavior is similar to amplifier H. Figure 8 shows scatter plots of the single pixel x-ray events versus column number (as would be used for serial CTI analysis), for readout through amplifier G and amplifier H, at the anomalously low value of $R\phi\_H = 7.0$ V. Clearly, the two halves of image section D respond quite differently at low $R\phi\_H$: while the section closest to amplifier G is well-behaved for all values of $R\phi\_H$, the section closest to amplifier H appears to suffer from hampered charge transfer from

the image section into the serial register, at Rϕ_H<8V. The corresponding images clearly show the charge trailing associated with this problem. For Rϕ_H>8V, this issue is completely resolved.

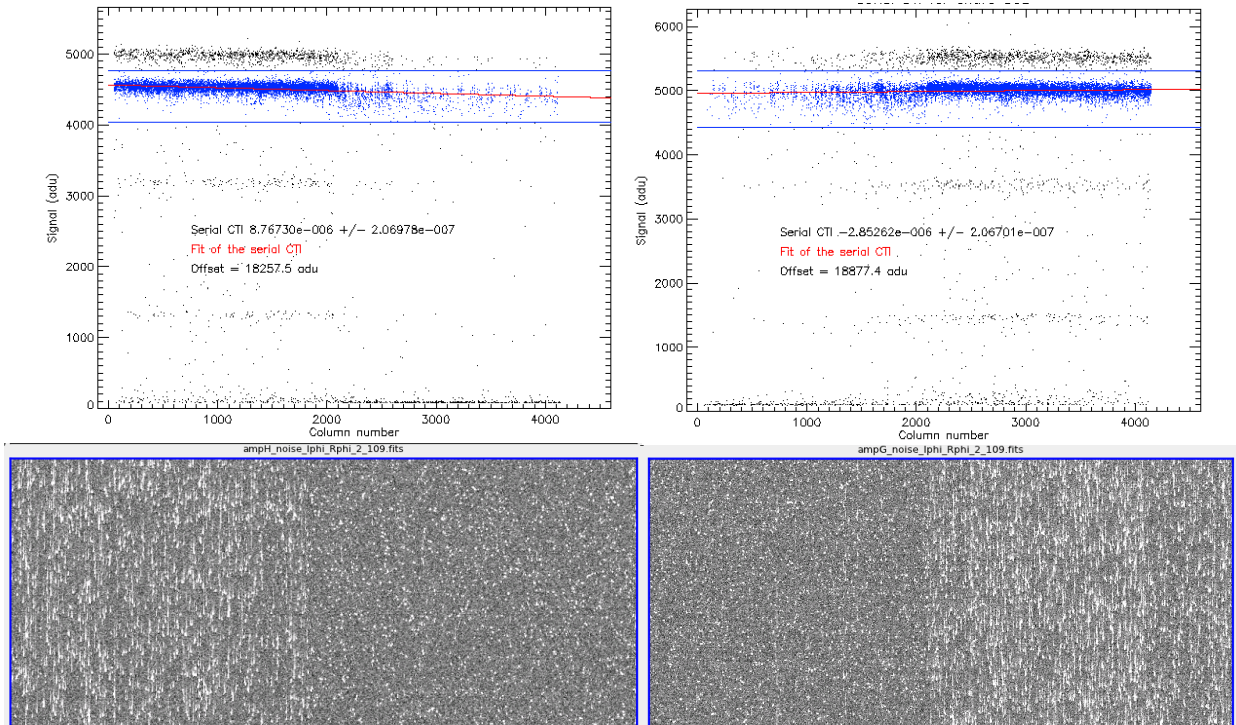Figure 8: Scatter plot of single pixel events from images read out through amplifier G (left) and H (right), with Iϕ_H=11.7V and Rϕ_H=7.0V. The panels below show a zoom-in of the images in the middle of the CCD. At this anomalously low Rϕ_H value, a hampered transfer of the charge at the image-to-register boundary occurs at the side of the H amplifier.

3.4 Noise versus pixel rate

With the optimized voltages (see 3rd column in Table 2) the dependence on the pixel rate of the read noise was measured by variation of the CDS integration time T_{int}. The results are shown in Figure 9. Measured noise values are plotted against CDS frequency, as well as against the resulting pixel rate. Note that at the high frequency end, pixel rate is very different from CDS frequency, due to the large overhead time of 3.5 µs in the pixel readout time. Hence, the noise performance at 200kHz pixel rate is strongly influenced by the overhead time in the pixel readout sequence, as this limits the available time for integration. The results have been corrected for the only known system noise contribution of 3.1 ADU rms. For comparison also the non-corrected values are shown (green line with triangle markers). The system noise has only a minor contribution to the measured noise, and only at the high frequency end. The reason for this is that, due to the fact that we have a Dual Slope Integrator, the signal increases proportionally to T_{int}, and hence a constant system noise in ADU becomes less important at low frequencies.

Finally, the noise from amplifier H was also measured with the serial clocks running in the reverse direction. This leads to a very different system offset. Since no x-ray signal are available from these images, the noise values in ADU were converted into electrons by using the conversion gain measurements from the measurements with proper clock direction. Results are shown in Figure 9, bottom panel, with purple X symbols.
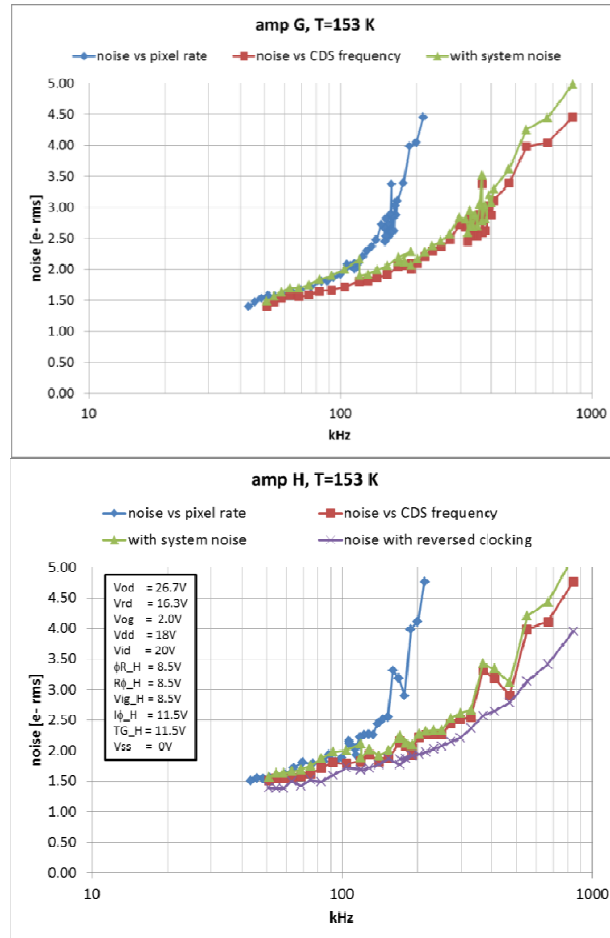
Figure 9: Noise versus pixel rate (and versus CDS frequency) with optimised clock and bias voltages for amplifier G (top) and amplifier H (bottom).

4.   CHARGE TRANSFER INEFFICIENCY

The charge transfer inefficiency (CTI) can be evaluated from the same series of x-ray images as used for the noise versus frequency measurements. This series has been complemented with similar series at other temperatures in the range 143-193 K (for amplifier H only). In addition, at T=143K a series of images with exposures times in the range 0.3-10 seconds was acquired in order to see the dependence of CTI on the amount of signal charge in the image. Bias and clock voltages were as in the 3rd column of Table 2. The results of these measurements are shown in Figure 10. The parallel CTI is found independent of pixel rate (as expected) and temperature, and amounts to $\leq 1 \times 10^{-6}$. The serial CTI shows a rather complex dependence on temperature and pixel rate. Therefore, the serial CTI has also been plotted as a function of temperature, for two pixel rates (70 kHz and 200 kHz). It is found that the serial CTI degrades with increasing temperature, up to ~175K. At higher temperatures, the dark current is starting to become significant and provides a background that fills traps, resulting in improved CTI. The curves for 70 kHz and 200 kHz are slightly shifted with respect to each other, in line with the observed temperature dependence. It should be noted, however, that we have changed the pixel rate only by changing the two CDS integration periods (see Figure 2), and not by 'stretching' the entire sequence. Therefore, the clock sequences at the two frequencies are not quite equivalent in terms of the relative charge dwell times under the three serial register phases. It has been found that the best CTI performance is achieved if the dwell times under all three phases are made equal [3]. This may also account for some of the difference in CTI between 70 and 200 kHz. The bottom right plot in Figure 10 shows the dependence of the CTI on the CCD exposure time, which is equivalent to the amount of signal charge in each image. For reference, all other measurements in Figure 10 were

taken at 2 seconds exposure time, which corresponds to 1 in 35 pixels carrying x-ray induced signal charge. As expected, serial CTI improves with increasing signal charge is the CCD.
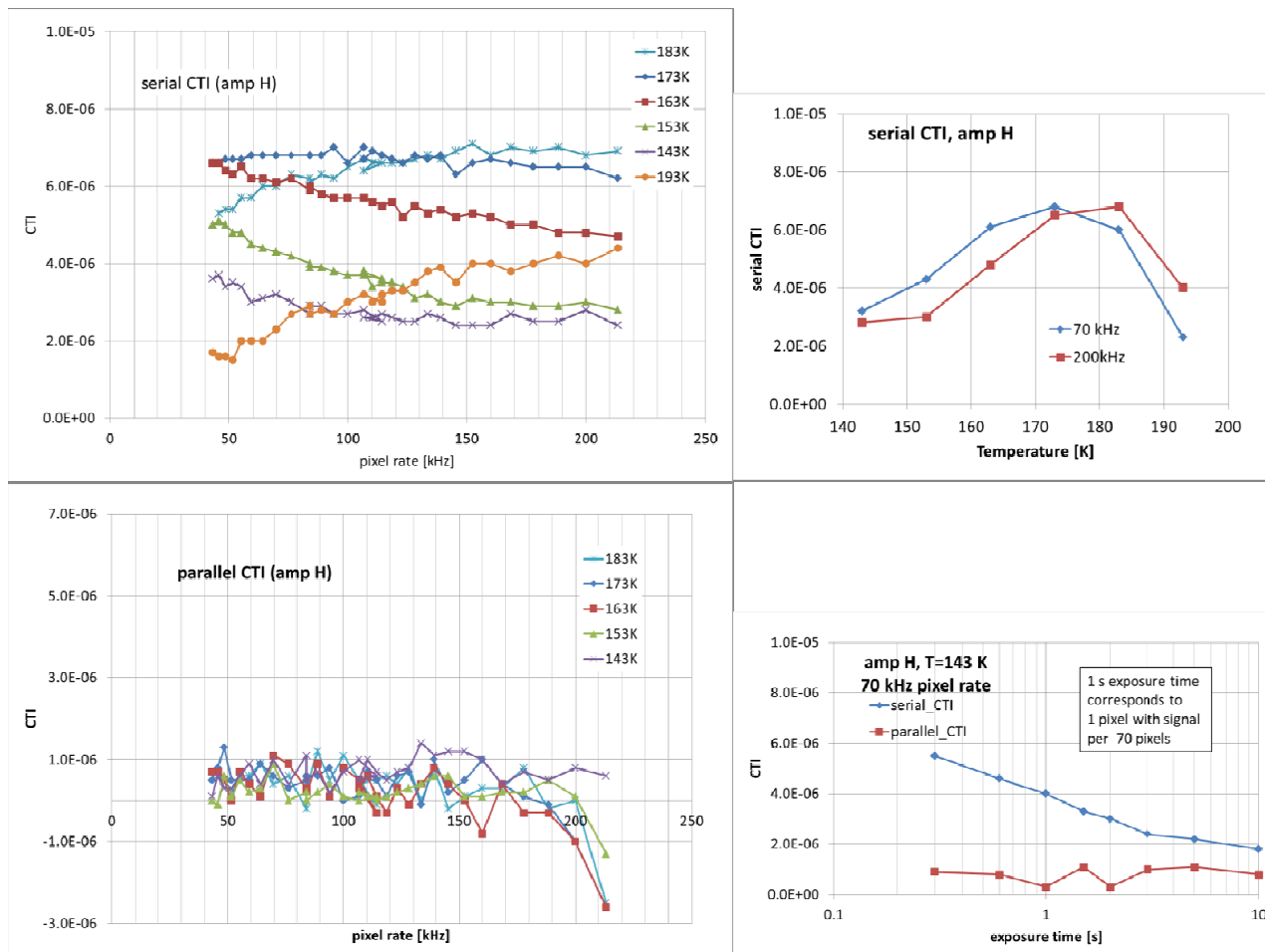

Figure 10: serial (top left) and parallel (bottom left) CTI versus pixel rate and temperature for readout through amplifier H.(T=153K, E= 5.9keV, ~1 pixel with signal above threshold per 35 pixels). Top right: serial CTI versus temperature for 70 kHz and 200 kHz pixel rate. Bottom right: CTI versus exposure time.

5.   DARK SIGNAL MEASUREMENTS

The dark current of the device was measured at temperatures in the range 150-210 K. At each temperature a series of dark images was recorded with 10x line binning, and at image integration times ranging from 0 to 3000 seconds. This allowed us to verify the linear dependence of dark signal on integration time, and evaluate the dark current from the slope of dark signal versus integration time curves. The results are shown in Figure 11, along with earlier results on a back-illuminated CCD204. Both devices follow the theoretical temperature dependence $I \sim T^{3/2} e^{(-E_{gap}(T)/2kT)}$, (with E_{gap} the temperature dependent band gap of Silicon), indicated with the dashed lines. The data follows the theoretical dependence down to ~170K. At the Euclid nominal operating temperature of 153K, the measured value is well below the required 6×10^{-4} electrons/s/pixel. We find about 2x lower dark current in the front-illuminated CCD273. It is not clear if this difference is related to the device being front-illuminated, or if it simply represents the variation between production batches. Alternatively, part of the difference may also be due to the temperature calibration in our set-up. The temperatures of the two devices were measured with different sensors, mounted on different parts of the packages, and also the packages of the two devices are quite different.

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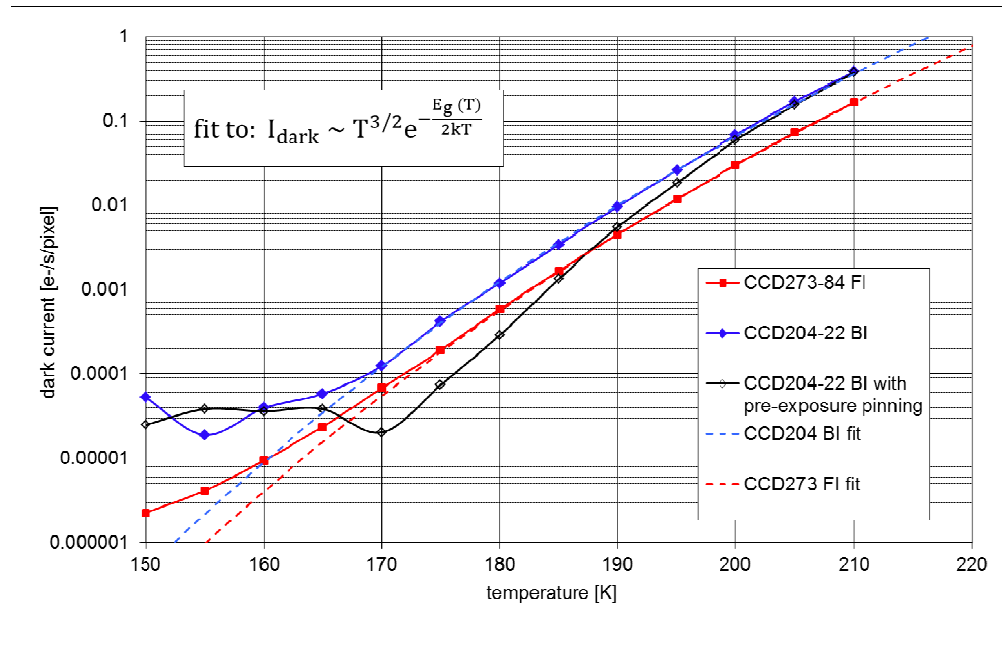

Figure 11: Dark current versus temperature for the prototype FI Euclid CCD273 (red squares). For comparison, dark current measurements on a BI CCD204 are also shown (blue diamonds). The dashed lines represent the theoretical temperature dependence, overlayed with the data. The black open diamonds represent measurements on the same CCD204, but obtained with a 2s pre-exposure pinning before each image integration.

The importance of verifying the linearity of dark signal with exposure time is illustrated with black curve and open diamond symbols in Figure 11, These data are from the same CCD204 as the blue solid diamonds, but obtained from images that were preceded by a short (2 s) pinning of the surface, achieved by raising the substrate voltage from 0 V to 9V. Such a pre-exposure pinning is very efficient in removing any residual surface image from previous exposures. However, depending on temperature it can take a long time before surface traps are filled again with surface dark signal charge. As a consequence these charges are not collected in the potential well and, hence, do not contribute to the dark signal. Therefore, for a finite time the measured dark current will be reduced, as seen in Figure 11. In fact, even after 3000 seconds of dark signals integration at temperatures as high as 200K, the dark current has barely reached the nominal value again. If we had derived the dark current from shorter integration times, the black curve would be found at even lower levels.

6.   SUMMARY

We have presented test results on a front-illuminated version of the Euclid prototype CCD273-82, obtained with our newly developed CCD test bench at ESA. Basic performance parameters such as noise, gain, charge transfer inefficiency and dark signal have been measured for two of the four amplifiers on the CCD. Both amplifiers show a wide range of bias voltages with constant noise performance. After optimisation of bias voltages and clock amplitudes, the noise levels at the baseline Euclid pixel rate was measured as 2.0 electrons rms, well within the Euclid requirement of 3.6 electrons rms. The charge transfer efficiency for parallel clocking is to $\leq 1 \times 10^{-6}$, without any dependence on temperature in the range 143-193 K. The serial CTI is dependent on temperature, pixel rate and amount of signal charge in the image. At the Euclid operating temperature of 153K and pixel rate of 70 kHz, the serial CTI is to $\sim 4.5 \times 10^{-6}$. The requirement for CTI is $\leq 5 \times 10^{-6}$. The measured dark current at T=153K is $< 1 \times 10^{-5}$ electrons/s/pixel, again well below the requirement of $\leq 6 \times 10^{-4}$ electrons/s/pixel. We will continue to test this device and its back-illuminated variant, when it becomes available. We will also test irradiated devices, with spot illumination to map the intra-pixel response, and to measure the change of spot shapes due to radiation damage.

ACKNOWLEDGMENTS

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