Characterization of HAWAII-2RG detector and SIDECAR ASIC for the Euclid Mission at ESA

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ABSTRACT

In the frame work of the European Space Agency's Cosmic Vision program, the Euclid mission has the objective to map the geometry of the Dark Universe. Galaxies and clusters of galaxies will be observed in the visible and near-infrared wavelengths by an imaging and spectroscopic channel.

For the Near Infrared Spectrometer instrument (NISP), the state-of-the-art HAWAII-2RG detectors will be used, associated with the SIDECAR ASIC readout electronic which will perform the image frame acquisitions.

To characterize and validate the performance of these detectors, a test bench has been designed, tested and validated.

This publication will present preliminary measurements on dark current, read noise, conversion gain and power consumption, In summary, the following results have been obtained in our system: dark current of 0.014 e⁻/s/pixel at 82K; readout noise of 23 e⁻ for a single CDS pair and 5.4e⁻ for a Fowler(32); a total electric power consumption of 203 mW in LVDS (excluding I/O power) mode.

The SIDECAR ASIC has also been characterized separately at room temperature. Two references voltages, VPreAmpRef1 and VrefMain, used to adjust the offset of the pre-amp DAC has been studied. The reset voltage, V_{reset} , was measured to have a root mean square stability of $22\mu V$ over 15 minutes and a root mean square stability value of 24 μV over a 15 hours measurement period. An offset between set value and measured value of around 60mV for low set voltages has been noticed. The behavior of VPreAmpRef1 and VrefMain with a adjustable external input voltage has been conducted in order to tune these two biases to cover the desired input range with the best linearity.

Keywords: Euclid mission, HAWAII-2RG, SIDECAR ASIC, characterization, ESA

1. INTRODUCTION

The infrared channel in the payload the Euclid satellite [1] will carry a focal plane consisting of a 4×4 array of HAWAII-2RG detectors with a cut-off wavelength at 2.5μ m.

The design of the satellite and final performances of the scientific mission will depend on detector performances such as dark current, readout noise and power consumption. To characterize and validate the specific performances of these detectors, a test bench has been designed, tested and validated.

Sections 2 and 3 of this publication are dedicated to the description of the cryogenic and the room temperature set up, respectively.

Results of conversion gain, dark current, readout noise, power consumption at cryogenic temperature are then shown in section 4.

In the last section, results obtained with the room temperature kit about bias voltage error and stability as well as the tuning of voltages such as the evolution of two internal reference voltages used in the DAC (VPreAmpRef1 and VRefMain) with gain will be presented.

2. CRYOGENIC TEST SET UP

The set-up consists of a HAWAII-2RG (S/N 224) $2k \times 2k$ pixel detector from Teledyne Scientific and Imaging [2] with a cut-off wavelength at 2.5 micron, together with a SIDECAR ASIC residing inside a liquid nitrogen cooled cryostat. The SIDECAR chip is connected to a JADE2 card located outside the vacuum vessel and operated at room temperature. The flex cable connection between the JADE2 card and the SIDECAR ASIC has been potted in a cryostat feedthrough.

The HAWAII-2RG detector is a state-of-the-art Near-Infrared (NIR) sensor consisting of an anti-reflection (AR) coated HgCdTe active layer, bump-bonded to a readout integrated circuit. A low noise source-follower circuit underneath each

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pixel and connected to multiplexers allows for a non-destructive readout scheme. Reference pixels, not sensitive to incoming light are present on the side of the detector to correct for any bias drift from the active region. The detector's 2048×2048 pixels can be read out through 1, 4 or 32 analog outputs. A window mode is also available to achieve faster readout rates.

The SIDECAR ASIC is designed to manage all aspects of imaging array operation and output digitization. It is composed of 36 analog to digital processing channels, 32 programmable digital I/O signals and 20 programmable bias voltages/currents. The preamplifier gain covers the range from -3dB to +27dB in 3dB steps in front of a slow 16 bit or fast 12 bit ADC. The data transmission between the SIDECAR and JADE2 card can be LVDS or CMOS. The JADE2 card serves as interface between a data acquisition computer and the SIDECAR chip.

In order to measure very low dark current reliably, a temperature stability in the mK range on the detector and SIDECAR ASIC is required. The detector and the SIDECAR are mounted on two different blocks controlled with two different Lakeshore temperature controllers achieving a mK range stability.

The cool down rate of the detector is done passively and has been designed to respect the cool down slope lower than 1K/min. The detector legs are screwed on a molybdenum plate to provide a good CTE match to the detector and good thermal conductivity.

Pictures of the detector on its molybdenum plate and the associated SIDECAR ASIC are shown Figure 1.



Figure 1 Left: Picture of the HAWAII-2RG detector on its molybdenum plate. Right : Picture of the SIDECAR ASIC

The detector can be illuminated via two LEDs (L10822 from Hamamatsu) with a peak emission wavelength at 1.3 micron. A photodiode (InGaAs, G8370 from Hamamatsu) placed near to the detector is used to control the relative illumination flux stability. Since these LEDs and photodiodes have been designed to work only down to -30C, a specific set up has been built to test them at lower temperatures. The results show that the LED and photodiode are still operational under vacuum and the required cryogenic temperature. Various cool down and warm up cycles were performed. Detailed inspection of the devices confirmed they did not suffer any damage from these cyclings.

A somewhat flat illumination based on light reflection from a detector cover is reached with this system. The complete set up is shown in Figure 2.

A separate dark (both optically as thermally) enclosure is used to cover the detector for dark current measurements.

The temperature control and data acquisition handling is achieved via a dedicated Python script that reproduces much of the functionality provided by the original Teledyne IDL application that was delivered with the detector assembly. The Python script interfaces to the sidecar COM interface using the "win32com" module. Visualization and analysis of data is achieved using the "matplotlib" and "scipy" modules. The Python script automates many procedures including: power on of the set-up, setting detector acquisition configuration, power measurements. It implements a fully automated data acquisition system for different temperature settings of the detector and the SIDECAR. Validation of the new software system was successfully done by comparing the telemetry and data output of the IDL and Python applications. A USB 2.0 port is used to interface the computer with the JADE2 board. To ensure a stable power supply, the JADE2 card is powered by an separate and external 5.5V power supply.



Figure 2 Overview of the system HAWAII-2RG SIDECAR ASIC

Before integrating the detector in its support, a molecular and particulate contamination tests has been performed. The particulate witness plate was placed in place of the detector and the molecular witness plate at the cold plate level. All steps required for detector operation, e.g. pumping, cooling down, warming up have been reproduced as if the detector was in place. The particulate contamination tests showed a result of 27 ppm, while the molecular contamination tests indicated a result of less than $0.2.10^{-7}$ g/cm².

These results are compliant with the Euclid contamination requirements (level 300 A/2), namely a particulate contamination lower than 100 ppm and a molecular contamination lower than 5.10^{-7} g/cm².

For the power consumption measurements, a PCB board has been designed and inserted between the JADE2 card and the flex cable to the SIDECAR. Current and voltage measurements of main biases are performed with a series of Keithley 2001 multimeters.

3. ROOM TEMPERATURE TEST SET UP

The test bench consists of the room temperature kit from Teledyne (SIDECAR development board, JADE2 card) and a specially designed PCB board. This PCB board, plugged instead of the detector is used to characterize the SIDECAR ASIC. This board allowed us to measure the biases supplied by the SIDECAR as also to feed the SIDECAR with a very stable voltage to characterize the ADCs.

The bias voltages supplied by the SIDECAR DACs are measured by a Fluke 8508A 8.5 digit reference multimeter. The SIDECAR ADCs bias are characterized using a very stable voltage calibrator Fluke 5440B

4. HAWAII-2RG DETECTOR AND SIDECAR CHARACTERIZATION

To achieve the scientific goals of the Euclid mission, the HAWAII-2RG detectors need to full fill specific requirements such as a dark current at 100K lower than 0.1e⁻/s/pixel. The tests presented in this section have been conducted at cryogenic temperature with a precise control of the temperature of the detector and the SIDECAR between 82K and 145K. The detector was run in the Euclid conditions, i.e. at 100KHz and using 32 outputs.

4.1 Conversion gain

The conversion gain is a key factor allowing the translation between the units coming out from the readout electronic (Analog to Digital Unit: ADU) to physical units, the photo-electrons accumulated in the detector.

The acquisition chain consists of the HAWAII-2RG detector and its readout electronic, the SIDECAR ASIC.

To validate the conversion gain measurement of the entire chain, the gain in ADU/V of the SIDECAR can be measured and compared to Teledyne test report. The global conversion gain (e/ADU) of the system will then be presented.

4.1.1 SIDECAR gain

The SIDECAR gain (ADU/V) has been computed by changing the input voltage of the SIDECAR (using the IDL software of Teledyne), acquire and then average frames. This operation has been done for each SIDECAR pre-amplifier gain. The median value over the resulting average frame gives the final result in ADU/V. The results showed in Figure 3, are in agreement with the Teledyne measurements.



As the gain of the SIDECAR has been validated, the conversion gain of the detector can now be computed. Similar results have been obtained on the room temperature kit using a hardware method (see section 5.3) instead of the Teledyne software method.

4.1.2 Detector conversion gain

The conversion gain is the factor allowing the translation of the signal coming from the readout electronic (in ADUs) into a physical unit, the corresponding number of collected electrons. The method used, based on Poisson statistics, is the photon transfer [3] method including the inter-pixel capacitance correction [4].

For a given current in the LED, 3 ramps constituted of 6 up the ramp frames are recorded. The signal recorded for each frame will increase during each ramp. After each ramp, the detector is reset and a new ramp can start. Each frame is corrected using reference pixels.

The correction algorithm based on the reference pixels is done in two steps and allows to remove common-mode noise and drift in the bias voltage.

The first steps is, for each channel, and for the odd and even pixels, to compute the mean of the top and bottom reference pixels. A clipped mean of 4 sigma is used to remove any hot or bad pixels in the distribution of the reference pixels. All pixels of the array are corrected by this first step. The second step is to use the lateral left and right reference pixels. A rolling average of eight pixels around each line "L" (four for each side, situated at the lines L-2, L-1, L+2, L+1) is computed.

The mean and the standard deviations for each illumination level are then computed based on the ramps' statistics.

The inter-pixel capacitance is measured using hot pixels in dark frames (see Figure 4). The advantage of using hot pixels is that they do not suffer from diffusion as there is almost no photo charge generated. The ratio between the signal in each pixel and the normalized sum give the value of the inter pixel capacitance. The average value of these coefficients are given in Figure 4

	0.63%	
0.61%	97%	0.60%
	0.64%	

Figure 4 Example of hot pixel with the inter-pixel capacitance with neighbour pixels and the average inter-pixel capacitance coefficients

The conversion gain with and without inter-pixel capacitance can be now computed (see Figure 5).



Figure 5 Photon transfer curve with and without inter-pixel capacitance

The conversion gain of the system SIDECAR with HAWAII detector is 3.82 e⁻/ADU. Knowing the gain of the SIDECAR set at 12dB or 72989 ADU/V) (see Figure 3) the gain of the detector is 3.58μ V/e⁻.

This gain will be used in all following results.

4.2 Dark current

The maximum allowed dark current level required for the Euclid mission is 0.1e/s/pixel at 100 K.

The dark current consists of charge carriers generated by thermal excitation.

The dark current generation process is dominated at high temperature by the generation-recombination process, which is proportional to $\exp(-E_g/nkT)$ with E_g the band gap energy of the detector, k the Boltzmann constant and T the temperature. At low temperatures, other phenomena such as the trap-to-band tunneling force the dark current to reach a plateau.

For each temperature of the detector, once it is stabilized to mK level, 60 ramps of 100 up the ramp frames have been taken. As previously explained, the reference pixels correction algorithm has been applied on each frame and a linear fit has been performed to find the dark current. The mean value of the slope for each ramp has been then computed.



Figure 6 Dark current evolution with temperature with n=1.8

The best fit has been obtained with a value of n=1.8. Clearly, the Euclid requirement of a dark current lower than $0.1e^{-1}$ /s/pixel at 100K is reached with this detector

4.3 Total readout noise

The readout noise is the uncertainty of the measured charge in a single pixel. Contributions to read noise include shot noise in the source-follower FETs, Johnson noise, 1/f noise, drifts in reference and ground voltages, etc.

The readout noise of the chain SIDECAR and HAWAII-2RG detector has been measured.

First the noise created by the SIDECAR has been quantified followed by the noise of the complete chain.

4.3.1 SIDECAR noise

The SIDECAR pre-amplifiers have 4 inputs, used for single-ended or differential scheme. The signal coming from the detector is connected to one of these input, named V2. Using internal multiplexers, these SIDECAR inputs can also be connected to pre-defined voltages. The noise created by the different operations taking place in the SIDECAR can then be measured by connecting the 4 inputs to analog ground. The noise performance of the SIDECAR was measured using CDSampling.

To compare with Teledyne's SIDECAR test report, tests have been performed with a gain of 13 (21dB) and a gain of 15 (27dB).

The results, illustrated in Figure 7, show a noise of $25\mu V_{rms}$ and $20.5 \mu V_{rms}$ for a gain of 13 and 15 respectively.

Teledyne measured a noise of 26.58 μ V_{rms} for a gain of 13 an 21.27 μ V_{rms} for a gain of 15. The gain of the SIDECAR in ADU/V computed in Figure 3 has been used to convert ADU into Volts.

The results show a good agreement with Teledyne's test report validating the low noise quality of the chain, power supply, JADE2 card and SIDECAR ASIC.



Figure 7 Left: Noise distribution of the SIDECAR with V1,V2,V3,V4 connected to analog ground for a gain of 13. Right: Noise distribution of the SIDECAR with V1,V2,V3,V4 connected to analog ground for a gain of 15

These results are compatible with the noise study realized by Markus Loose [5] at T=37K who reported (for a same gain of 15) a median noise of 25 μ V_{rms}.

4.3.2 Detector and SIDECAR readout noise

To measure the total noise of the acquisition chain, the Fowler(N) [6] acquisition scheme was used.

Ramps of 2 groups of 32 frames with a constant integration time between corresponding Fowler pair frames, has been recorded.

A standard middle gain of 8 (12dB) has been used as it will reduce the ADCs contribution to the digitization noise and allow the full dynamic range of the detector to be utilized.

Each frame of Fowler(N) has been corrected by the reference pixel correction algorithm described in section 4.1.2.

For each ramp, the difference D of the mean of N frames between the two Fowler groups has been computed. The noise results from the temporal standard deviation of the difference D for each pixel. A detector map of the temporal noise is then obtained.

To verify any systematic in the temporal noise analysis, the spatial noise has been compared to the temporal noise. For a CDS sampling, the spatial standard deviation has been compared to the temporal standard deviation given by 60 ramps of CDS.

The distribution over the entire array (see Figure 8) of the temporal noise of all CDS ramps shows a noise of 23 e⁻ for the active pixels.



Figure 8 Right: Spatial CDS distribution of the active pixels with a standard deviation of 24e⁻. Left: Temporal noise for CDS frames for active pixels showing a mean of 6.02ADU or 23e⁻.

The pixel distribution of a single CDS sampling (see Figure 8) indicates a readout noise (based on spatial statistic) of 24e⁻.

The results show the same level of noise between the two methods and prove the temporal noise stability of our system. By comparison, the theoretical CDS noise can be computed using the test report of Teledyne and the noise of the SIDECAR alone.

Teledyne performs the CDS detector noise measurement by replacing the SIDECAR by a very low noise readout electronic. The noise of the detector itself can be derived to give a value of 12.86e⁻ for a CDS.

The SIDECAR noise for the same ADC gain has been measured to a value of 13.6e⁻. The theoretical total noise (detector and SIDECAR) can be computed using the quadratic sum of the two noise components to give a final value of 18.6e⁻.

The readout noise reduction obtained by increasing the number of frames for each Fowler can now be computed.

A sampling of 60 ramps of Fowler(32) with a constant time of 240s between corresponding frames has been used.

The detector was operated at a stable temperature of 82K resulting in a negligeable impact of the shot noise from dark current.

A temporal analysis has been performed over 60 ramps and the result is shown in Figure 9. The theoretical curve is based on the noise reduction with a factor $1/\sqrt{N}$, where N is the number of frames.



Figure 9 Noise diminution with number of Fowler frames

The total noise decreases to a value of 5.4^{e⁻} of Fowler(32). The distribution of the active and reference pixels for the Fowler(32) are shown in Figure 10.



Figure 10 Fowler 32 noise distribution for the active and reference pixels reaching a noise of 5.4e

4.4 HAWAII-2RG and SIDECAR power consumption

The electrical power consumption of the detector and SIDECAR will impact the thermal heat load and so the requirements for the thermal design of the instrument. The digital interface between SIDECAR and JADE2 can be configured in two different modes, LVDS and CMOS which has an effect on the SIDECAR power consumption and heat load. The electrical power consumption has been measured in both modes.

To measure the total power consumption of the detector and the SIDECAR, a PCB board has been designed and fitted between the JADE2 card and the flex cable going to the SIDECAR (see Figure 11)



Figure 11 PCB board allowing power consumption measurement situated between the JADE2 card and the flex cable to the SIDECAR

This PCBoard allows to extract, at the same time, current and voltage of main SIDECAR supplies e.g. V_{dda} , V_{ddd} , V_{dd3p3} and $V_{ddl/O}$. The power consumption has been measured in two cases, using CMOS and LVDS data transmission respectively.

In CMOS mode, the total power consumption is given by the sum of the power consumption of V_{dda} , V_{dd3p3} . The power consumption on V_{ref} line, not accessible with our board, has been verified with the Teledyne software to be lower than 0.1 mW. This voltage is not included in our total reported electrical power consumption.

For the LVDS mode, the situation is more difficult because of the current flowing on the differential signals line which is dissipated into heat in the 100 Ω termination resistors in front of the LVDS receivers. Following this, in LVDS mode, it is necessary to split the electric power supply consideration from the SIDECAR thermal considerations. Some of the power on the V_{ddl/O} and V_{ssl/O} lines is burned in the JADE2 card LVDS receivers. On the other hand, the current driving the SIDECAR LVDS inputs is not measured on the power supply lines. Because we don't have details on the SIDECAR LVDS implementation we can't specify yet the precise thermal heat load of the SIDECAR.



Voltage	Voltage	Current	Power
name	(V)	(mA)	(mW)
V _{dda}	3.2722	48.8.	159.6
V_{ddd}	2.4722	65.3	16.1
V _{dd3p3}	3.2681	86	28.1
V _{ddI/O}	2.6307	99.6	262.0
Total			465.9

The plot in Figure 12 shows the electrical power consumption in LVDS and CMOS mode, with these caveats.

Figure 12 Electrical power consumption in CMOS and LVDS mode and the detailed table for 32 outputs in LVDS mode

5. SIDECAR ASIC ROOM TEMPERATURE CHARACTERIZATION

In view of characterizing the SIDECAR alone in cryogenic environment, we first used the room temperature kit to evaluate the circuit's performance. In the near future, these measurements will be repeated in the cryogenic set up. To characterize the SIDECAR and its influence on the complete chain, some measurements are made on the 92 pin connector which is normally used to connect the detector ROIC. The measurements described here are made on the room temperature kit in a clean lab environment at room temperature to prepare for the cryogenic measurements. No detector or ROIC was connected at this stage.

5.1 SIDECAR room temperature test bench

The SIDECAR test bench is composed of the room temperature SIDECAR ASIC board connected to the JADE2 card and linked to a computer by a USB interface. An Agilent power supply provides the operating voltage of 5.5V to the JADE2 card. A small PCB with a 92 pin connector is mounted on the SIDECAR board instead of the detector flex cable. This board offers access to the SIDECAR DAC output channels 0 and 3. In the Teledyne development kits these channels are used for V_{reset} and V_{biaspower}. The reason for choosing these two biases was that V_{reset} is one of the biases which is not connected to decoupling capacitors on the board and V_{biaspower} is filtered with a combination of 47μ F+1 μ F+1 μ F decoupling capacitors. This choice allows to evaluate the impact of the decoupling capacitors on the noise. It is anticipated that these two biases are representative for the other ones. On the board there is also a SMA female connector which is wired to the ADC channel 15 input for ADC characterization. Reference for all measurements is AGND. The photo Figure 13 shows the mounted PCB.



Figure 13 Measurement connection board connected on SIDECAR instead of HAWAII-2RG detector

5.2 Bias voltage error and stability

The purpose of this test was to evaluate the error between the bias set via the Teledyne software and the real value created on the SIDECAR. Temporal stability of the bias has been also evaluated. These error and drift can impact the data quality as they are used for each ramp of the science acquisition.

The SIDECAR offers several analogue outputs to provide operating, reference and bias voltages for the detector. These voltages are generated by digital to analogue converters (DACs), and are adjustable using the software tools provided by Teledyne. Measurements of the DAC voltages are made using an $8\frac{1}{2}$ -digit reference multimeter Fluke 8508A. We connected the multimeter to one of the DAC outputs where normally the detector or ROIC would be connected. In these measurements the only load for the SIDECAR output is the capacity of the wires and the high input impedance of the voltmeter.

5.2.1 Bias Voltage Error

With the Teledyne software the voltage of V_{reset} , linked to DAC channel 0, was set in steps of 100mV over both ranges, 0V to 2.0V and 1.3V to 3.3V. The corresponding output voltage was measured with the Fluke 8508A. For every step an average over 25 measurements was calculated.

Both, the low-end and the high end of the voltage range could not be reached. With the setting 0V the output provides 63mV, with the setting 3.3V the output reaches 3.223V. For lower range values the output is always around 60mV higher than the set value. This results in a high relative error for low voltages, e.g. 21% error for a set value of 0.3V(see Figure 14), which is the default value for V_{reset} for the HAWAII-2RG detector.



Figure 14 Relative voltage error room temperature kit DAC channel 0 (Vreset)

5.2.2 Bias Voltage Stability

To determine the short term stability and long term drift the DAC voltage was measured over time.

In the Euclid framework, the longest exposure time for the Near Infrared Spectrometer instrument, using the HAWAII-2RG detector is around 540s (or 9 minutes) in a Fowler mode sampling. The stability over 15 minutes (short term) and 15 hours (long term) with a Fowler ramp of 540 s have been recorded.

The short term measurements are made in 6.5 digit mode (Filter=on, Fast=off) of the Fluke 8508A resulting in around 1.6 measurements per second. Over the first nine minutes of this measurement the SIDECAR was running a Fowler ramp after this it was idling.

Figure 15 shows the result for V_{reset} set to 0.301V and the corresponding histogram. The dark bars represent the measured distribution, the light ones are the overlaid expected Gaussian curve. The mean is about 0.360765V and the standard deviation about 22.4 μ V.

For V_{reset} set to 3.3V, we can notice (see Figure 16) a drift and larger variations during the first nine minutes when the acquisition ramp was running.

To detect long term drifts, measurements over 15 hours were performed. For these measurements the Fluke voltmeter was set in 8.5 digit mode (Filter=on, Fast=off) with voltage logging every 30.1 seconds. Figure 17 shows the result for V_{reset} set to 0.301V with overlaid Gaussian curve.

From all the measurements the following rms noise on V_{reset} were calculated (see Table 1)

Voltage : Vreset (V)	0.301	3.3
rms noise for short term measurement	22µV	87µV
rms noise for long term measurement	24µV	63µV

Table 1 rms noise on V_{reset} for long and short term measurement

The reason for the higher value at 3.3V short term measurement is expected from the noisy behaviour while sampling an image.

The rms noise for a gain of 8 for V_{reset} =0.301V (default value in the Teledyne test report) will result in a noise around 2 ADU. For the highest gain, it will create a noise of 8 ADU using a direct translation volt to ADU of the ADC for a gain of 12dB.



Figure 15 Left: Short term measurement, Vreset set to 0.301V, 1 ramp of a Fowler mode during 540s was sampled. Right: the associated histogram and the associated Gaussian



Figure 16 Short term measurement, V_{reset} set to 3.300V, 1 ramp of a Fowler mode during 540s was sampled



Figure 17: Long term measurement (15 hours), Vreset set to 0.301V, signal distribution and Gaussian overlay

5.3 ADC Input Voltage Range

For image acquisition, the SIDECAR offers 32 analog inputs. Each of them can be sampled with a fast 12 bit analog to digital converter (ADC) or a slower 16 bit ADC. Given the Euclid framework, measurements were performed using the 16 bit ADCs.

To determine the influence of different reference voltages and gain settings on the input voltage range which can be sampled, an external adjustable precision voltage source was connected to input channel 15 of the SIDECAR. For this purpose the SMA connector of Figure 13 was connected to a Fluke 5440B voltage calibrator in low voltage (divider) mode configuration. In several configurations the input voltage was swept in steps of 100mV or smaller if necessary. The ADU value was determined as the mean over 1 million samples (pixels).

Figure 18 shows the influence of variation of $V_{preAmpRef1}$. It is noticeable that the default value of 1.2512V for this bias voltage results in a kind of saturation effect at the low end. Lower values for $V_{PreAmpRef1}$ seems to be preferable.



Figure 18: ADC Input Range for Gain 8 (12dB, large Cint), $V_{RefMain} = 1.6031V$ depending on $V_{PreAmpRef1}$

With $V_{PreAmpRef1}$ set to 0.5005V for a more linear behaviour, the influence of the gain setting was measured. Figure 19 shows the results for gain settings of 1 (0dB), 4 (6dB, large C_{int}), 8 (12dB, large C_{int}) and 15 (27dB, large C_{int}). From the measurements the transfer gain was calculated in Table 2.

Gain	Transfer gain (ADU/V)
1 (0db)	19183 ADU/V
4 (6dB, large C _{int})	38321 ADU/V
8 (12 dB, large C _{int})	75501 ADU/V
15 (27dB, large C _{int})	380927 ADU/V

Table 2 Calculated transfer gain in ADU/V



Figure 19: ADC Input Range for $V_{PreAmpRefl} = 0.5005V$, $V_{RefMain} = 1.6031V$ depending on Gain setting

Figure 20 shows the influence of variation of $V_{RefMain}$. To cover the low input voltages with high linearity, the optimal set of voltage is given by $V_{PreAmpRef} < 0.750V$ and finalizing the tuning by adjusting $V_{refMain}$ given the Figure 20.



Figure 20: ADC Input Range for Gain 8 (12dB, large Cint), $V_{PreAmpRef1} = 0.05005V$ depending on $V_{RefMain}$

In this study, optimal values of $V_{refMain}$ and $V_{preAmpRef1}$ have been determined to give the maximum linearity and cover the desired input voltage range. The measurements will be repeated on the cryogenic set-up once available.

5.4 ROIC and SIDECAR power consumption

The power consumption of the RT-kit is very close to the consumption measured at cryogenic temperature.

6. CONCLUSION

We have designed and tested a new test bench for the HAWAII-2RG and SIDECAR characterization in the frame work of the Euclid mission.

The conversion gain has been measured using the photon transfer curve and the hot pixels used to determine the interpixel capacitance. A value of 3.82e⁻/ADU has been found taking into account 0.6% of inter-pixel capacitance for each of the 4 neighbouring pixels. The dark current has been measured down to a value of 0.01e⁻/s/pixel at 82K. The readout noise of the SIDECAR alone and then the entire detector and SIDECAR chain has been also measured. The SIDECAR noise has been compared to and found in agreement with the Teledyne test report while the detector noise for a single CDS pair has been measured to be 23e⁻. Using Fowler sampling, a noise of 5.4e⁻ for a Fowler(32) has been achieved. The electrical power consumption in CMOS and LVDS configuration has been calculated to be 318mW in CMOS mode and 203 mW in LVDS mode (without I/O) for 32 channels.

The SIDECAR ASIC has been characterized at room temperature using the room temperature kit. The bias voltage offset and stability has been tested on V_{reset} showing a deviation up to 65% between the set and measured voltage value, particularly in the lower range. Concerning the long term and short term stability, we noticed that the frame acquisition process perturbs the stability of the bias. For a gain of 8 (12dB), the rms noise for the default value of V_{reset} ($V_{reset} = 0.301V$) give a noise of 2 ADU using a direct translation volt to ADU

The study of the behavior of $V_{PreAmpRef1}$ and $V_{refMain}$ allow to adjust these two biases to give the best linearity and cover the desired input range value.

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