In 2019, Eurospace and ESA agreed to form an ECSS WG with the objective to change, update and improve the existing ECSS-Q-ST-60-02C “ASIC and FPGA Development” standard to reflect the evolution and changes in ASIC and FPGA technology since the publication of the present standard 10 years ago. The main users, European companies and institutions developing Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to be used on-board missions had identified multiple shortcomings and gaps when applying the standard.

The number and scope of the changes proposed by Industry, CNES and ESA was such, that the ECSS WG decided to supersede ECSS-Q-ST-60-02 with the creation of an engineering in the ECSS-E-ST-20 family, and a dedicated PA standard in the ECSS-Q branch.

The WG agreed to address evolution for both ASIC’s and FPGA’s manufacturing processes, along with the methods and tools for their design and test and to undergo a major revamp to reflect all the technological changes for engineering but also Product Assurance. The goal was to address the fast evolution of ASICs, the increase in complexity of today’s but also tomorrow’s System-on-Chip (SoC) (including FPGA technology), the dependency on external software programmes (hence creating the need for HW-SW co-engineering design for ASIC/FPGA embedding microprocessor cores as well as general requirements for IP cores (re)use), but also state-of-the-art Product Assurance and Safety processes including tailoring of the standard according to the different ASIC/FPGA type but also the precise scope of use of the development based on criticality.