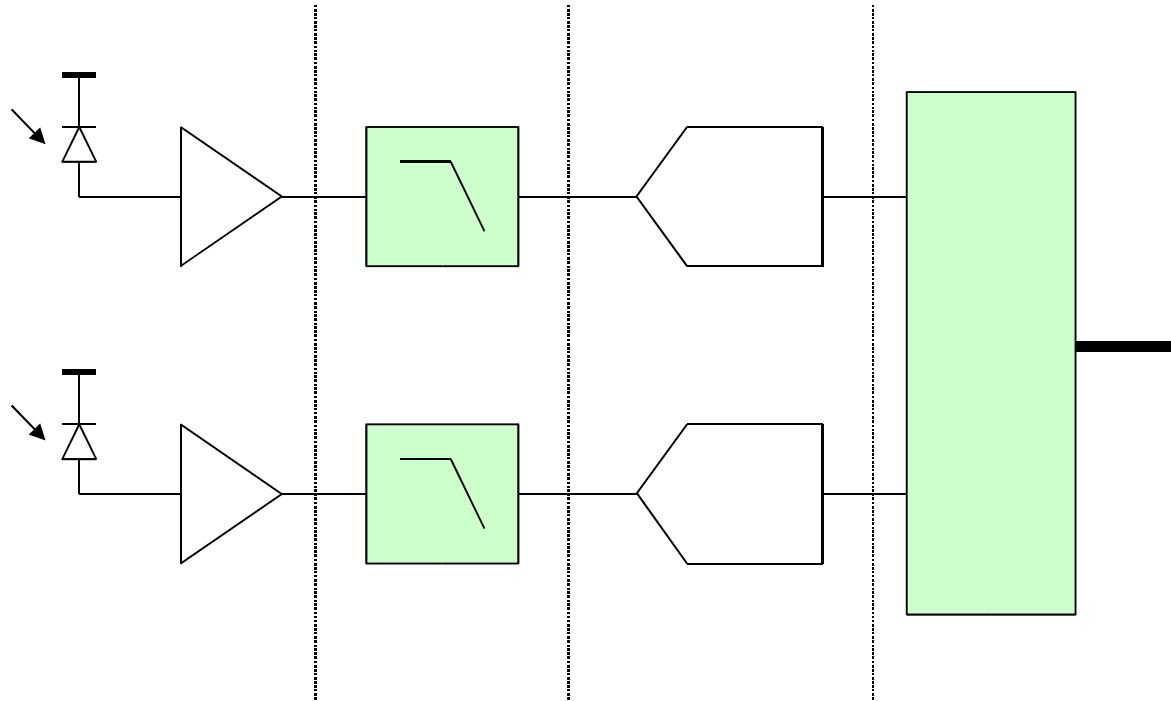# Implementation of the Phasemeter for LISA Pathfinder

S.Aston, D.M.Hoyland, A.M.Cruise

University of Birmingham

Schematic

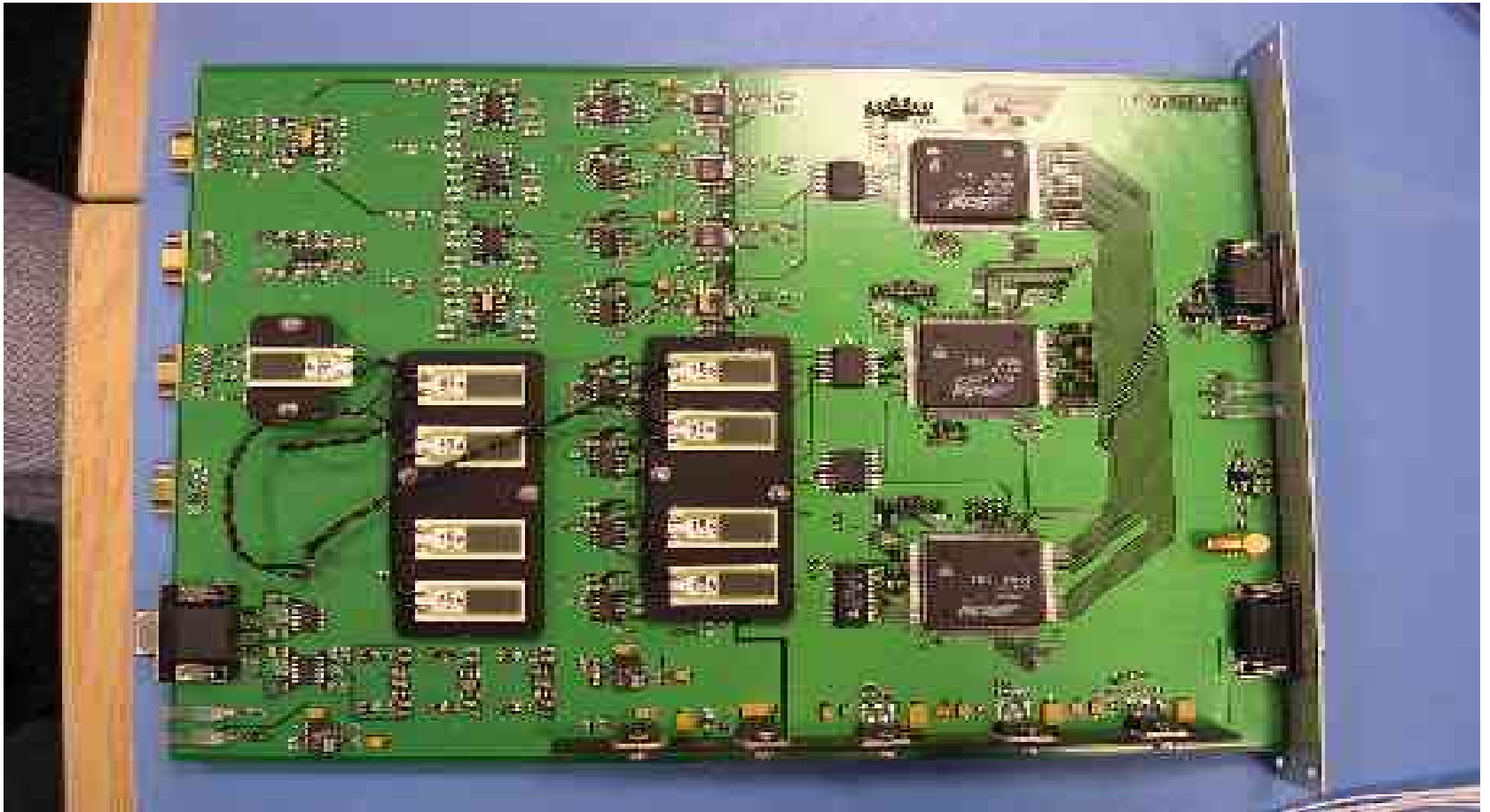Photodiode   Trans-impedance Amplifier   Filter   ADC   Processing and interface
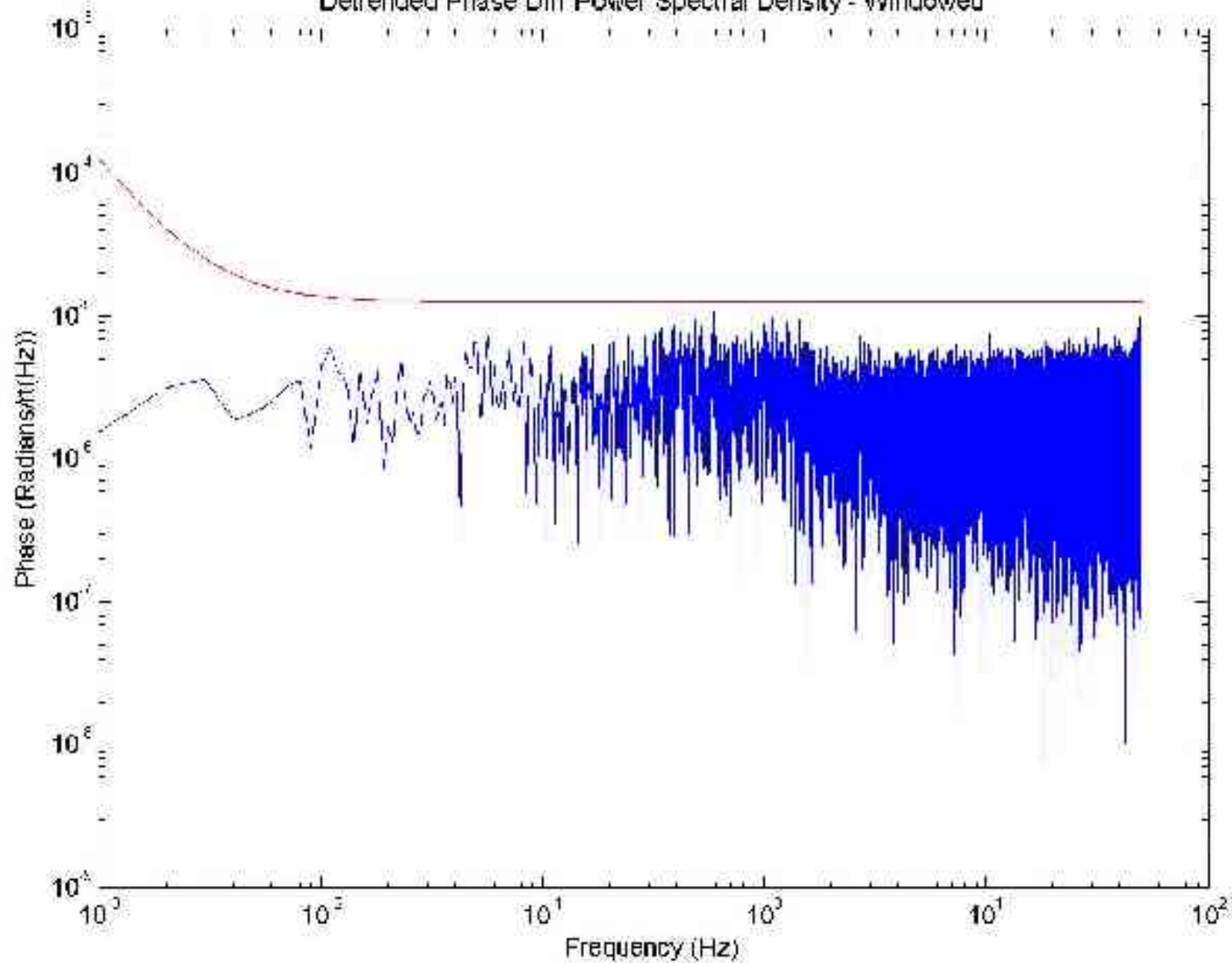
X 16

Physical Implementation

Testing in Progress

Detrended Phase Diff Power Spectral Density - Windowed

Transimpedance amplifiers

- Signal levels to accommodate 0.5 mW require trans-impedance of ~ 4KΩ

- OP484 chosen for Lab and flight models

- Input current < 0.4pA/root Hz

- Bandwidth in excess of 300kHz

- Total gain for system contained in op-amp

- Rad hard to 100krad

- Same component used for filters

Anti-aliasing filter

- Protection against aliasing noise into sampling frequency range
- Temperature stability extremely important and 0.25 C/root Hz has been assumed
- 110db of rejection needed at 50kHz
- 7th order Tchebychev filter
- Filter roll off at 12.8 kHz
- Uses OP 484

Digitisation

- About 14 bits of digitisation needed
- AD7676 provides 16 bits
- Settle time of 1-2µs
- Dwell time of 20µs
- Digitisation noise of 3.0 10^{-6} rads/root Hz
- Digitization rate of 50 kHz chosen
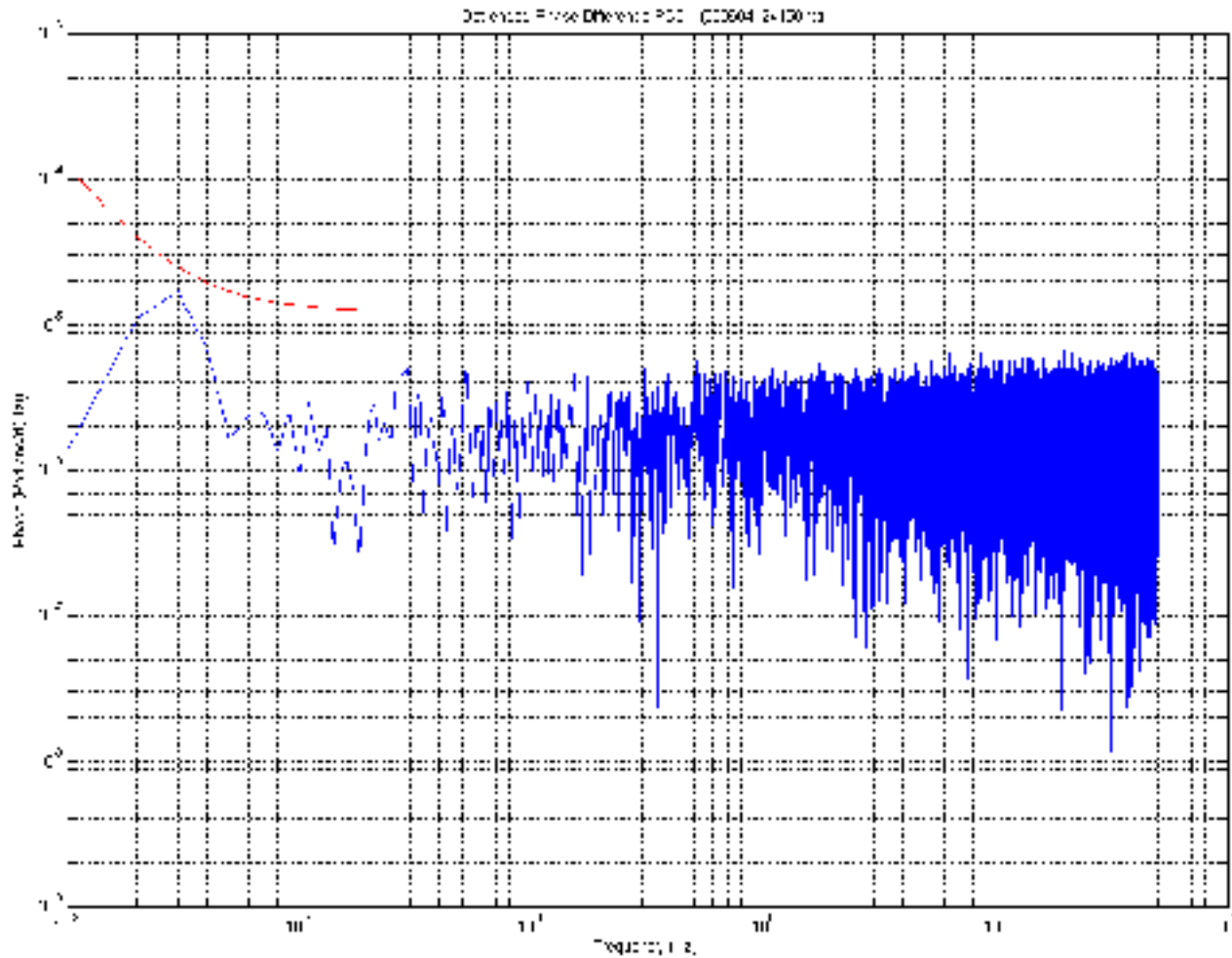- Power limitations important
- Timing jitter in ADC is important

Clock Noise

SMART-2: 10MHz Clock Reference Source
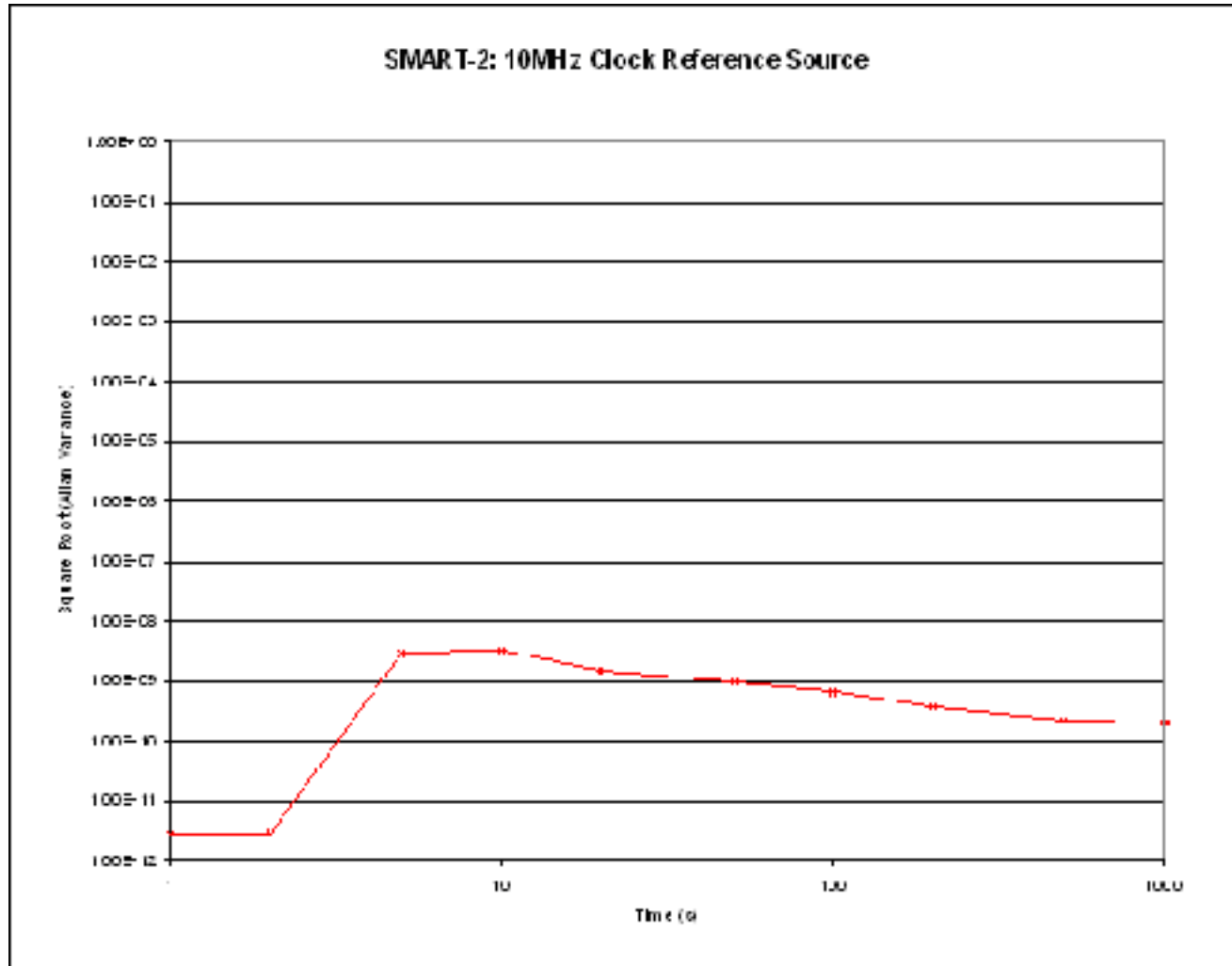
Single Bin Fourier Transform

- Carried out in FPGA
- Sine and Cosine tables programmable from ground
- FPGA programmable in circuit
- Sample rate 0.1 to 1.0 Hz

Stimulated Temperature effects

Preparations for LISA LTP

- Conversion of prototype to Flight Model now funded by PPARC

- Programme shows schedule contingency of > 1 month

- Technical performance demonstrates margin of x6

Acknowledgements

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